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Analysis Switching Pulse of DC Level Shifting Modulating Technique in Multilevel Inverter

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ABSTRACT

Multilevel Inverters (MLI) is contemplating in an attempt to optimize the ripple content and voltage stress across power semiconductor devices. This breakthrough is an essential aspect for a high power and medium voltage applications. In this work, Modulating technique is analyzed and designed to synthesize maximum level at the output. The proposed DC level switching technique is used on cascaded topology is designed to reduce total harmonic distortions in output AC waveform. The detailed analysis is done on 9-level (line-line) with continuous AC sinusoidal waveform. This 9-level is achieved by cascading two basic cells in series. The topology used can be extended for N level by using (3N-3)/2 switches and (N- 1)/4 dc sources. DC level shifting technique consists of reference sinusoidal wave and carrier DC levels. The Number of DC carrier levels depends on the number of levels generated. When sinusoidal wave is greater than dc level a pulse is generated at the output .This techniques is beneficial as compared with other modulating technique as it does not require high frequency carrier waveform. The analysis of switches is evaluated with software results. The software results are validated using MATLAB/SIMULINK. The total harmonic distortion (THD) using modulating DC Level shifting technique is found to be 10.41 %.

***Keywords**: DC Level Shifting, Ripple, Total Harmonic Distortion, Cascaded MLI.*

Introduction

In a recent year power electronics conversion devices plays a vital role in various renewable, traction, automotive and high and medium voltage applications [1]. The increase of the world energy demand has entailed the appearance of new power converter topologies and new semiconductor technology capable to drive all needed power [2]. The current energy arena is changing due to dependence on fossil fuels and the progressive increase of its cost is leading to the investment of huge amounts of resources, economical and human, to develop new cheaper and cleaner energy resources not related to fossil fuels. Since decades, renewable energy resources have been the focus for researchers and different families of power inverters have been designed to make the integration of these types of systems into the distribution grid a current reality. Besides, in the transmission lines, high-power electronic systems are needed to assure the power distribution and the energy quality. Among various Power conversion devices Multilevel Inverter gain attention in energy conversion devices. The commonly used conventional MLI topologies include Diode-Clamped (DC-MLI), Flying Capacitor (FC-MLI), and Cascaded H-Bridge (CHB-MLI) structures [3]. Among these, the Cascaded H-Bridge inverter has gained significant attention in renewable energy applications due to its modular structure, inherent reliability, and the absence of clamping diodes and floating capacitors. Based on the magnitude of input DC sources, CHB-MLIs [4] are categorized into symmetrical and asymmetrical configurations. So far work is carried out on various MLI topologies, among that cascade MLI is mostly used due to less number of switching devices and DC sources used as compared to another topology of MLI. The CHB topologies [5],[7]-[8] are proper option for more number of level applications from point of view of modularity and simplicity of control.

In addition to topology design used in cascaded topology, modulation techniques play a crucial role in determining the performance of MLIs. Various modulation strategies have been developed to achieve high-quality output voltage and reduced harmonic distortion. Common techniques include Sinusoidal Pulse Width Modulation (SPWM), carrier-based methods such as Phase Disposition (PD), Phase Opposition Disposition (POD), and Alternate Phase Opposition Disposition (APOD), as well as advanced approaches like Space Vector Modulation (SVM) and Selective Harmonic Elimination (SHE)[9]-[10],[12].

In this paper, a DC level shifting modulation technique is employed to generate the required switching pulses for the proposed MLI topology [6]. This technique is selected due to its simplicity, ease of implementation, and capability to produce multiple voltage levels with reduced harmonic distortion. Additionally, it facilitates better control of switching devices and improves overall system performance. The main advantage of this modulating technique is the Total harmonic content is also reduces as compared to other techniques. In this modulating technique carrier wave that is DC levels generated is compared with reference wave that is sinusoidal wave. After comparison when reference wave is greater than carrier wave a switching pulse is generated and the detailed analysis of pulse is shown in this paper.

Proposed Work of DC level Modulating Technique

In proposed work modulating DC level shifting modulating technique is used and the pulses obtained are given to switches of proposed cascaded topology.

The topology of multilevel inverter employs cascaded arrangement of two basic cells is shown in Figure 2.1. This MLI is designed, where nine output levels is obtained by twelve switches S_1-S_{12} and four symmetrical dc sources V_{dc1}-V_{dc4}. It is possible to introduce a new cascaded multilevel inverter by using a series connection of n basic units. As number of output levels is increased, output approaches close to sinusoidal waveform. The output voltage obtained from basic cells of MLI are shown by $V_{O1}$and V_{O2}.The output voltage (V_{out}) of the proposed cascaded multilevel inverter is shown in equation (1).Further by introducing the n basic cell in series the voltages can be extended for n output voltage as shown in equation (2).

$$V_{out}=V_{O1}+V_{O2} \quad (1)$$

$$V_{out}= V_{01} + V_{o2} + \cdots + V_{on} \quad (2)$$

For the topology, the number of switches (N_{switch}) and dc voltage sources(N_{source})are written by the following equations(3)and(4),respectively

$$N_{switch}=6B \quad (3)$$

$$N_{source}=2B \quad (4)$$

Where, B is the number of basic cell.

For the magnitudes of dc voltage sources having symmetrical configuration given in equation (5), the number of output voltage levels (N_{Level}), maximum magnitude of the producible output voltage levels ($V_{o,max}$ are evaluated by the following equations (6)and (7).

$$V_{1,j}=V_{2,j}=V_{dc} \text{ for } j=1,2,3\ldots\ldots n \quad (5)$$

$$N_{level}=4B+1 \quad (6)$$

$$V_{o,max}=2B \quad (7)$$

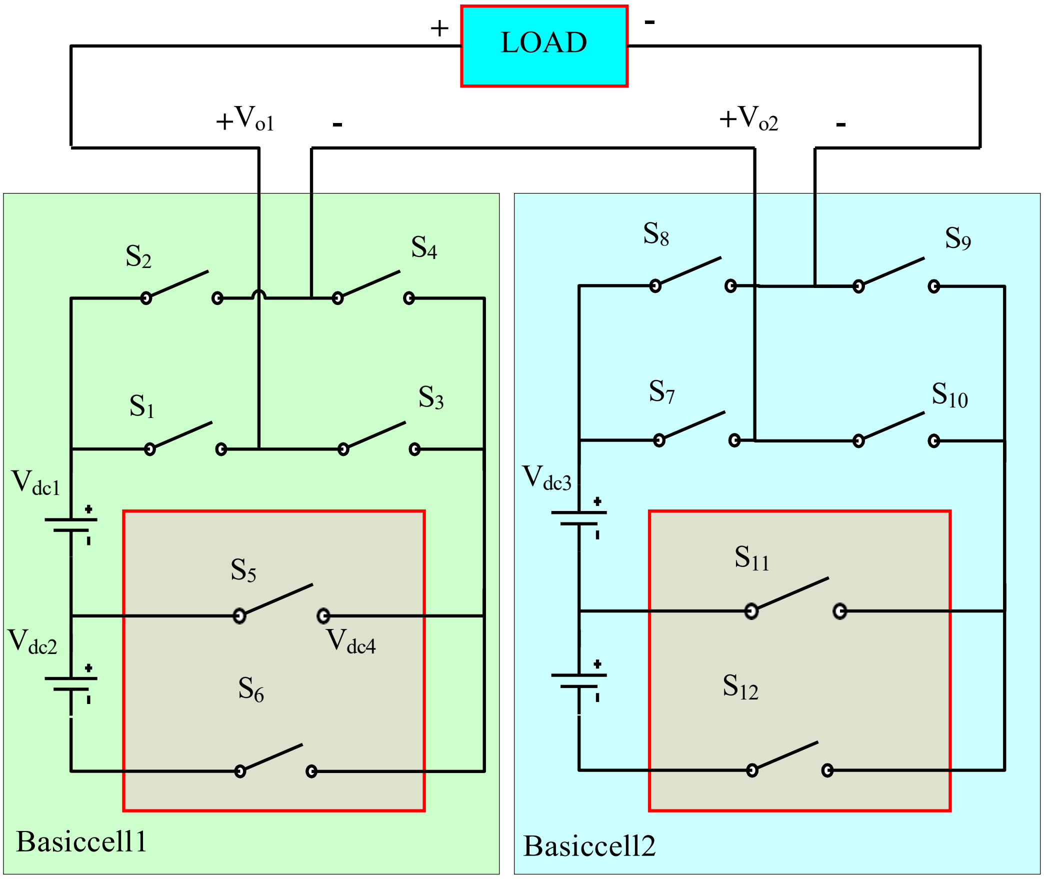

Figure 1: Cascaded MLI with twelve switches

- **Generation of Switching Pulses**

The switching states to trigger the H-bridge containing switches and auxiliary network containing switches of cascaded MLI topology is shown in Table 2.1. The time T_{OFF} with delay of 60ns is required so that the turn ON switches can be turn OFF, and the time of T_{ON} with delay of 50ns is needed so that the turn OFF switches can be turned ON based on the type of these switches.

Table 1: Switching states of MLI

Switching states												Voltage Levels
S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	
1	0	0	1	0	1	1	0	1	0	0	1	**$(V_1+V_2+V_3+V_4)$**
1	0	0	1	0	1	1	0	1	0	1	0	**$(V_1+V_2+V_3)$**
1	0	0	1	0	1	0	0	1	1	0	0	**(V_1+V_2)**
1	0	0	1	1	0	0	0	1	1	0	0	**(V_1)**
0	0	0	0	0	0	0	0	0	0	0	0	**0**
0	1	1	0	1	0	0	0	1	1	0	0	**$-(V_1)$**
0	1	1	0	0	1	0	0	1	1	0	0	**$-(V_1+V_2)$**
0	1	1	0	0	1	0	1	0	1	1	0	**$-(V_1+V_2+V_3)$**
0	1	1	0	0	1	0	1	0	1	0	1	**$-(V_1+V_2+V_3+V_4)$**

The switching pulses to bridge 1 of proposed topology are generated by comparing sinusoidal waveform with the dc levels(V_{dc1},V_{dc2},$-V_{dc1}$,$-V_{dc2}$).When sinusoidal wave is greater than dc level pulse is generated at the output. As shown in Figure 2.2 to obtain output voltage waveform of five levels (L-L) from bridge 1 with delay count following steps of operation to trigger switches are given below-

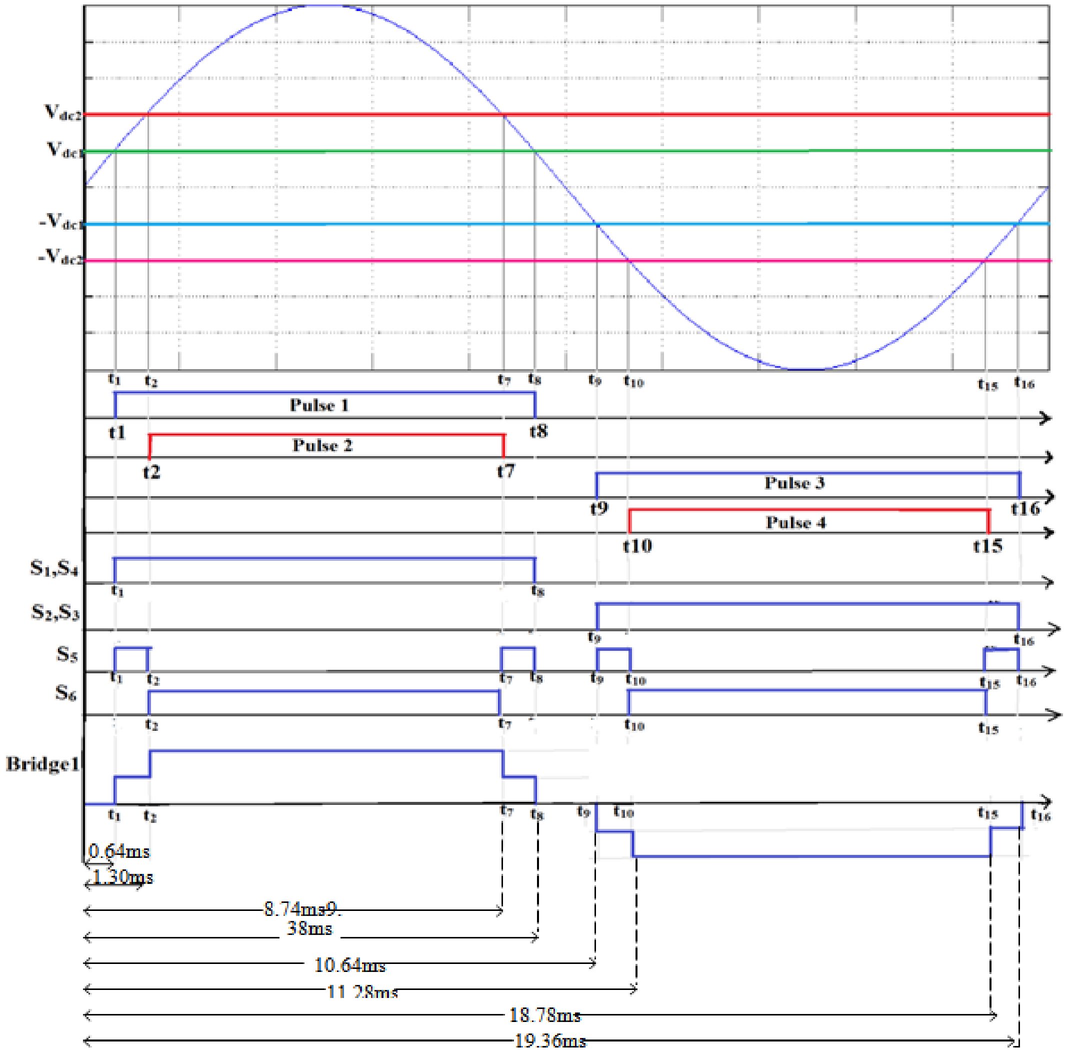

Figure 2: Generation of switching pulses to bridge 1

- To trigger switches S_1 and S_4, pulse 1in the interval (t_1-t_8) ranging from (0.64ms-9.38ms) with a delay of 0.64ms is provided.
- To trigger switches S_2 and S_3, pulse 2 in the interval (t_9-t_{16}) ranging from (10.64ms-19.36ms) with a delay 10.64ms is provided.
- To trigger switch S_5, initially to generate pulse in positive cycle pulse 2 is complemented and is ANDed with pulse 1, the resultant obtained isR_1.Further to generate pulse in negative cycle pulse 4 is complemented and is ANDed with pulse 3, the resultant obtained is R_2. The two resultant R_1 and R_2 are ORed to obtain switching pulse S_5 with delay 0.64ms.For example switch is made ON and OFF made with delay count as shown in Figure 2.3.

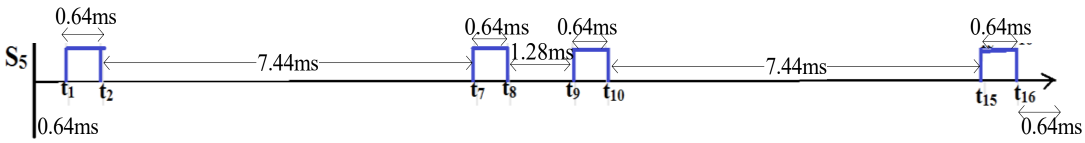

Figure 3: Switching pulse for switch S_5 with delay count

- To trigger switch S_6, the Pulse 2 and Pulse 4 are ORed with delay 1.30ms.

The switching pulses to bridge 2 of proposed topology are generated by comparing sinusoidal waveform with the dc levels (V_{dc3}, V_{dc4}, $-V_{dc3}$, $-V_{dc4}$).As shown in Figure 3.15 to obtain output voltage waveform of five levels (L-L) from bridge 2 with delay count following steps of operation to trigger switches are given below-

- To trigger switches S_7, pulse 5 in the interval (t_3-t_6) ranging from (2.04ms- 8.2ms) with a delay of 2.04ms is provided.
- To trigger switches S_8, pulse 7 in the interval t_9-t_{12} ranging from (10.64ms- 12.52ms) with a delay 10.64ms is provided.
- To trigger switch S_9, to generate pulse in negative cycle pulse 8 is complemented and is ANDed with pulse 7, the resultant obtained is R_2. The resultant R_2 and pulse 5 obtained during positive cycle are ORed to obtain switching pulse S_9 with delay 2.04ms.
- To trigger switch S_{10}, to generate pulse in positive cycle pulse 6 is complemented and is ANDed with pulse 5, the resultant obtained is R_1. The resultant R_1 and pulse 7 obtained during negative cycle are ORed to obtain switching pulse S_{10} with delay 2.04ms.
- To trigger switch S_{11}, initially to generate pulse in positive cycle pulse 6 is complemented and is ANDed with pulse 5, the resultant obtained is R_1.Further to generate pulse in negative cycle pulse 8 is complemented and is ANDed with pulse 7, the resultant obtained is R_2. The two resultant R_1 and R_2 are ORed to obtain switching pulse S_5 with delay 2.04ms.
- To trigger switch S_{12}, thePulse 6 and Pulse 8 are ORedwith delay2.95ms.

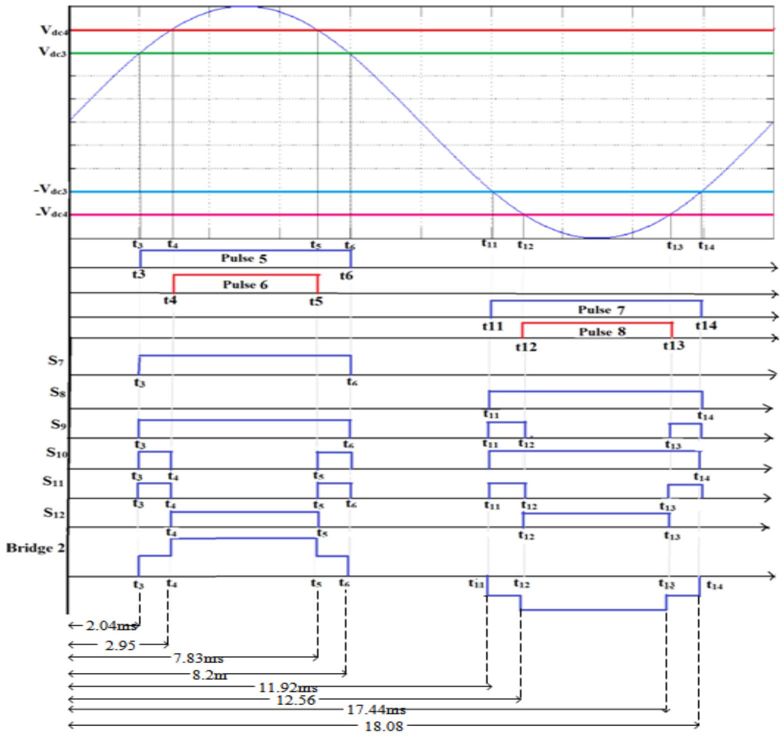

Figure 4: Generation of switching pulses to bridge 2

When bridge 1 and bridge 2 are cascaded in series with output voltages of (V_{01}+V_{02}) and (V_{03}+V_{04}) are added together to achieve final output voltages of (V_{01}+V_{02}+V_{03}+V_{04})with nine levels(L-L)across proposed MLI as given in Figure 2.5. The operation of the proposed MLI for nine levels is illustrated from the switching states in Table 2.1.

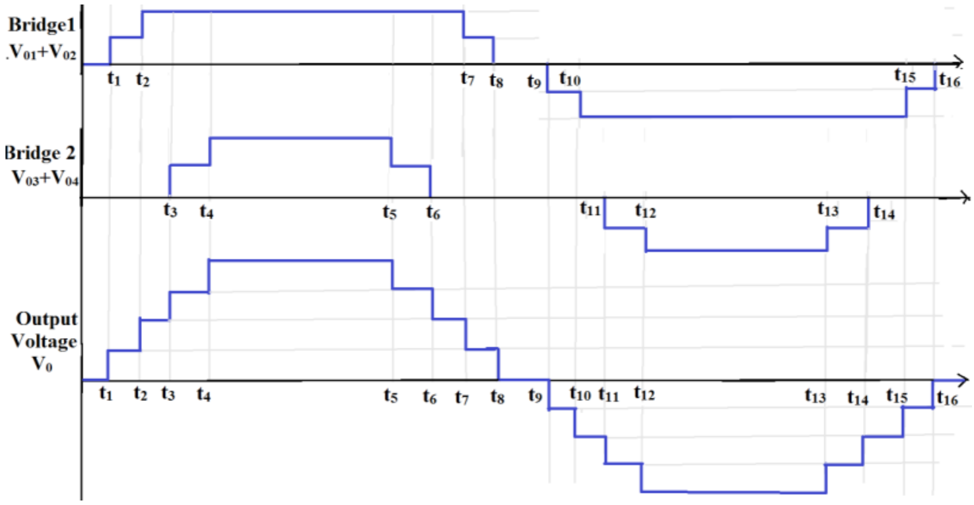

Figure 5: Resultant output voltage waveform

The switching pulses to trigger the switch is programmed in microcontroller using ATMEL studio .The twelve pins of port D and port B is utilized to drive the twelve switches of proposed cascaded topology. The Figure 6 shows the switching pulses for respective positive and negative levels.

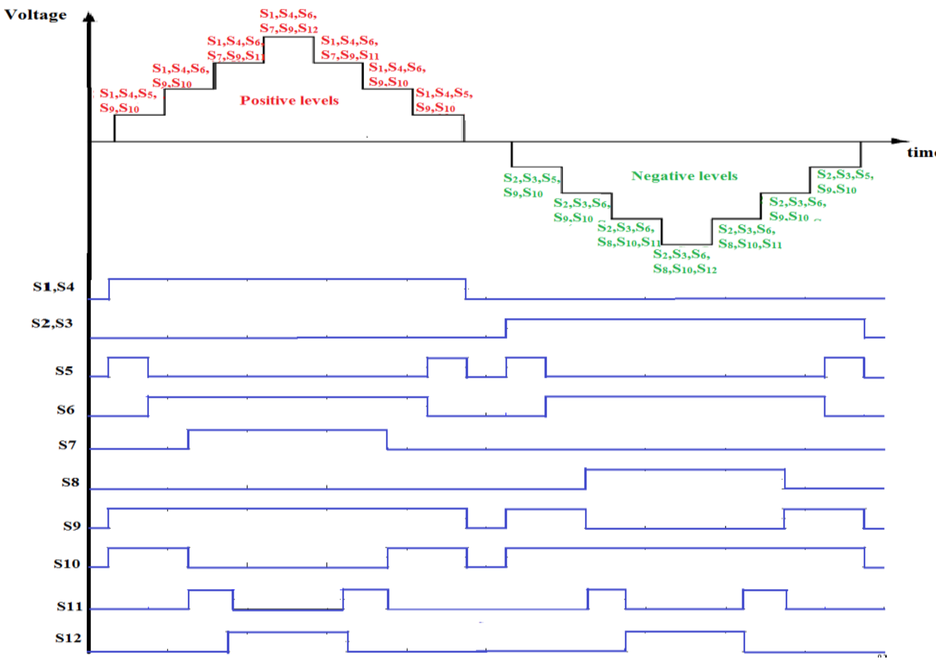

Figure 6: Switching pulses for respective positive and negative levels

Conclusion

The cascaded topology using dc level shifting technique helps to obtain higher output levels with fewer semiconductor devices with minimum standing voltage on switches for realizing N_{step} for the load. There is reduction of installation area, cost, and complexity. The performance index which includes quality factor THD 10.41% are analyzed and determined from simulation results. The number of switching devices had reduced when compared with the conventional methods. Considerable improvement in the harmonic factor had reduced the size of the passive filter. Also it is found that H-bridge of proposed topology possesses higher voltage stress than the complementary switches. These confirmatory results are verified by MATLAB/SIMULINK simulation and analysis of each output step with DC level shifting technique is done. It is found that DC level shifting technique is more advantageous than other PWM techniques.

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